Remarks

Claims 2, 6-8, 50 and 57 have been amended. Support for these amendments is found in the specification and drawings, and thus no new matter has been added. Claims 25-36, 47, 49, 51, 53-56 and 63 are pending in the present application.

Rejection under § 103

Claims 2, 6-8, 25-36, 47, 49-51, 53-58 and 60-63 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al (US 6,507,098) in combination Suzuki et al (US 5,532,910). The Examiner asserts that Lo et al. teach all the limitations of the independent claims except, "at least one decoupling capacitor conductively coupled to at least one of said first and second semiconductor dies or wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of one of said first semiconductor die, said second semiconductor die, or a topographic contact. The Examiner further asserts that Suzuki et al. utilizes a decoupling capacitor accommodated in a space coupled to a die and concluded that it would have been obvious to one of ordinary skill in the art to incorporate a decoupling capacitor into the modified package including Lo in order to remove noise as taught by Suzuki et al. (Col. 1, line 48).

Applicants respectfully traverse the rejection of the claims and submit that the burden of establishing a prima facie case of obviousness under §103 has not been met. *MPEP §2145.* In order to establish a prima facie case of obviousness under §103, the Examiner has the burden of showing, by reasoning or evidence, that: 1) there is some suggestion or motivation, either in the references themselves or in the knowledge available in the art, to modify that reference's teachings; 2) there is a reasonable expectation on the part of one of ordinary skill in the art that the modification or combination has a reasonable expectation of success; and 3) the prior art references (or references when combined) teach or suggest all the claim limitations. *MPEP §2145.* The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Independent claims 2, 6-8, 49, 50, and 57 recite a multiple die semiconductor assembly comprising, *inter alia*, a first semiconductor die, a second semiconductor die, an intermediate substrate positioned between the first semiconductor die and the second semiconductor die, and a

decoupling capacitor mounted to a first surface of the substrate, wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of either the first semiconductor die or a topographic contact extending between the intermediate substrate and the first semiconductor die.

Applicants respectfully submit that neither Lo et al. nor Suzuki et al. teach, suggest, or motivate, singularly or in combination, a decoupling capacitor mounted to an intermediate substrate within a stacked chip arrangement, wherein a thickness dimension of the capacitor is accommodated by a space defined by a thickness dimension of either a first semiconductor die or a topographic contact extending between the substrate and the first semiconductor die. As acknowledged by the Examiner, Lo et al. do not disclose or suggest a decoupling capacitor, let alone a capacitor mounted to an intermediate substrate and conductively coupled to one of the first and second semiconductor dies, wherein a thickness dimension of the capacitor is accommodated by a space defined by a thickness dimension of either the semiconductor die or topographic contact. In fact, the only reference applied by the Examiner that does disclose a capacitor is Suzuki et al. (Lo et al. is all void of any such teaching or suggestion regarding capacitors).

However, Suzuki et al. teach the capacitor is mounted on a lead frame so as to be connected in series with the output terminals of a IC chip and sealed in mold resin (22). (Col. 1, lines 48-50). Nowhere does Suzuki et al. teach or suggest, singularly or in combination with Lo et al. or any other reference, a capacitor mounted to an intermediate substrate and conductively coupled to one of first and second semiconductor dies, wherein its thickness dimension is accommodated by a space defined by a thickness dimension of either the first semiconductor die or a topographic contact that extends between the substrate and the die.

To alleviate this deficiency in the prima facie case, the Examiner stated, "With respect to the placement of the capacitor, such that a thickness dimension of said decoupling capacitor accommodated in a space defined by a thickness dimension of one of said first semiconductor, it would have been obvious, since the rearrangements of parts have been held unpatentable absent a showing of criticality or unexpected results." *In re Japikse*, 181 F.2d 1019, 86 USPQ 70 (CCPA 1950); see also *In re Kuhle*, 526 F.2d 553, 188 USPQ 7 (CCPA 1975). However, "The mere fact that a worker in the art could rearrange the parts of the reference device to meet the terms of the claims on appeal is not by itself sufficient to support a finding of obviousness. The

prior art must provide a motivation or reason for the worker in the art, without the benefit of appellant's specification, **to make the necessary changes** in the reference device." (emphasis added) *Ex parte Chicago Rawhide Mfg. Co.*, 223 USPQ 351, 353 (Bd. Pat. App. & Inter. 1984); see also MPEP §2144.04 (VI)(C). Additionally, the Federal Circuit has stated, "The mere fact that prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. It is impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious." *In re Fritsch*, 23 USPQ2d 1780, 1783-4 (Fed. Cir. 1991).

Applicants respectfully submit that the prior art provides no such required motivation or reason to mount the capacitor of Suzuki et al. on the substrate of Lo et al., let alone such that a thickness dimension of the capacitor is accommodated in a space defined by a thickness dimension of either the first semiconductor die or a topographic contact extending between the substrate and die as recited by Applicants claims. Both Suzuki et al. and Lo et al. are silent, singularly or in combination, as to mounting capacitors in such a stacked chip arrangement, particularly wherein its thickness is accommodated by a space defined by either the first semiconductor die or topographic contact. Moreover, neither reference, singularly or in combination, teach or suggest the capacitor conductively coupled to either the first or second semiconductor dies. These are explicitly claimed limitations that the Examiner has not shown as taught explicitly or implicitly in the art. Lacking the necessary teaching, motivation, or suggestion, Applicants respectfully submit that the Examiner has arbitrarily made the necessary changes in the reference devices to come up with Applicants' claimed invention. Thus, Applicants believe the Examiner has mistakenly used Applicants' specification as a "template" to piecemeal the teachings of the prior art to reject Applicants' independent claims.

Moreover, as set forth above, Suzuki et al.'s capacitor is connected in series to the IC chip's output terminals. In sharp contrast, Applicants' claim 8 recites that the capacitor is coupled between high and low voltage inputs of either the first or second semiconductor die. Applicants respectfully submit that Suzuki et al.'s capacitor connected to output terminals does not teach or suggest the capacitor connected between high and low voltage inputs as recited by Applicants' claim 8.

Therefore, Applicants respectfully submit that the none of the references, singularly or in combination, teach or suggest all of the limitations of Applicants' claims 2, 6-8, 49, 50, and 57. Accordingly, the required burden of a prima facie case of obviousness has not been met and the Applicants respectfully request that the rejections under 35 U.S.C. §103 of independent claims 2, 6-8, 49, 50, and 57 be withdrawn. As claims 25-36, 47, 51, 53-56, and 63 depend from independent claims 2, 6-8, 49, 50, or 57, the rejection of these claims under 35 U.S.C. §103 should be withdrawn as well. Thus, the Applicants respectfully submit that, in view of the above amendments and remarks, the application is now in condition for allowance. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully requested.

Respectfully submitted,
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